Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-17. (Canceled).

18. (Currently Amended) A method for data processing in an integrated circuit having cells, the cells adapted for executing programs, comprising:

running a first program;

in response to a waiting condition during which no program execution is able to take place, saving data from the cells to a memory;

running a second program after the data is saved; and

reloading the saved data into the cells after running the second program;

wherein the second program tests the cells to detect a defective cell.

19. (Previously Presented) The method of claim 18, wherein the waiting condition is one of a wait cycle and an IDLE cycle.

20. (Previously Presented) The method of claim 19, wherein a duration of the second program corresponds to a duration of the one of the wait cycle and the IDLE cycle.

21. (Canceled).

22. (Previously Presented) The method of claim 19, further comprising:

running a third program before reloading the data if, after running the second program, the one of the wait cycle and the IDLE cycle has not completed.

23. (Previously Presented) The method of claim 18, wherein the memory is one of a chip-internal and a chip-external memory.

24. (Previously Presented) The method of claim 18, wherein the data is saved and reloaded only if the data will be used subsequent to running the second program, and wherein the second program is run without saving the data if the data will not be used subsequent to running the second program.

25. (Canceled).

26. (Previously Presented) The method of claim 44, wherein the cells are configurable cells and the data includes configuration data.

27. (Previously Presented) The method of claim 44, wherein a duration of the test routine program corresponds to a duration of the one of the wait cycle and the IDLE cycle.

28. (Previously Presented) The method of claim 44, wherein the memory is one of a chip-internal and a chip-external memory.

29. (Previously Presented) The method of claim 44, wherein the data is saved and the saved data is loaded only if the data will be used subsequent to running the test routine program, and wherein the test routine program is loaded onto the cells without saving the data if the data will not be used subsequent to running the test routine program.

30. (Currently Amended) A method for data processing in an integrated circuit having cells, the cells adapted for executing programs, comprising:

loading a first data onto the cells;

running a first program on the cells with the first data;

during one of a wait cycle and an IDLE cycle, removing the first data from the cells;

subsequent to removing the first data, loading a second data onto the cells;

running a second program on the cells with the second data;

subsequent to running the second program, removing the second data from the cells; and

subsequent to removing the second data, reloading the first data onto the cells;

wherein the second program tests the cells to detect a defective cell.

31. (Previously Presented) The method of claim 30, further comprising:

connecting a first plurality of registers to the cells in order to load the first data;

connecting a second plurality of registers to the cells in order to load the second data;

disconnecting the first plurality of registers from the cells in order to remove the first data;

disconnecting the second plurality of registers from the cells in order to remove the second data.

32. (Previously Presented) The method of claim 30,

wherein loading the data further comprises transmitting the data to a plurality of registers;

wherein removing the first data further comprises transmitting the first data from the plurality of registers to a memory location; and

wherein removing the second data further comprises loading the first data.

33. (Previously Presented) The method of claim 32, wherein the first data is transmitted from the plurality of registers to the memory location only if the first data will be used subsequent to running the second program.

34. (Previously Presented) The method of claim 30, wherein the memory location is one of a chip-internal memory location and a chip-external memory location.

35. (Previously Presented) The method of claim 30, wherein a duration of the second program corresponds to a duration of the one of the wait cycle and the IDLE cycle.

36. (Previously Presented) The method of claim 30, further comprising:

running a third program on the cells if, after running the second program, the one of the wait cycle and the IDLE cycle has not completed.

37. (Canceled).

38. (Currently Amended) An integrated circuit, comprising:

a plurality of cells configured to execute programs; and

a memory for storing data,

wherein:

the plurality of cells is configured to save the data to the memory when a first program enters a waiting condition, to execute a second program after the data is saved, and to retrieve the data after the second program is executed; and

the second program tests the cells to detect a defective cell.

39. (Previously Presented) The integrated circuit of claim 38, wherein the plurality of cells includes at least one configurable cell, and the data includes a configuration data.

40. (Previously Presented) The integrated circuit of claim 38, wherein the memory is one of a chip-internal and a chip-external memory.

41. (Previously Presented) The integrated circuit of claim 38, wherein the second program is configured to test the plurality of cells for a defective cell.

42. (Previously Presented) The integrated circuit of claim 45, wherein the plurality of cells is configured to execute a third program if, after the second program is executed, the one of the wait cycle and the IDLE cycle has not completed.

43. (Previously Presented) The integrated circuit of claim 45, wherein a duration of the second program corresponds to a duration of the one of the wait cycle and the IDLE cycle.

44. (Previously Presented) The method according to claim 18, wherein the second program is a test routine program, and wherein the waiting condition is one of a wait cycle and an IDLE cycle.

45. (Previously Presented) The integrated circuit of claim 38, wherein the waiting condition is one of a wait cycle and an IDLE cycle.

46. (Previously Presented) The integrated circuit of claim 38, wherein the second program is a test routine program.